

In the specification:

Please amend the paragraph beginning at page 7, line 2 as follows:

*C1*  
The control signal 19 received on the input 37 may be divided into two distinct signals 63 and 64. The signal 63 may bias the drain terminal of the transistor 59, and the signal 64 may bias the drain terminal of the transistor 69 to drive the inverter circuit 53 to generate an output 77, which serves as the input for the next delay cell 28.

Please amend the paragraph beginning at page 7, line 18 as follows:

*C2*  
Fig. 5 is a timing diagram illustrating an example of phase delays produced by the synchronous clock generator 8. The clock signals 13 (CLOCK) and 14 ( $\overline{\text{CLOCK}}$ ) may be complimentary and may have substantially the same period ( $T$ ). The data signal 12 (DATA) received on the channel 5 may also have the same period as the signals 13 and 14. Fig. 5 also shows that the output signal 23 ( $\text{CLOCK}_{\text{Delay}}$ ) and the output signal 24 ( $\overline{\text{CLOCK}}_{\text{Delay}}$ ) may be delayed by a period ( $T_L$ ) relative to the input clock signals 13 and 14. The delay permits the data signal 12 to be latched on a rising edge 79 of the clock signal 23 13 or the rising edge 80 of the clock signal 24 14 at a time ( $T_L$ ), after the transient time ( $T_{\text{trans}}$ ) of the signal 12.